Conference Name: EnSci Sydney 2024 – International Conference on Engineering & Sciences, 24-25 April
Conference Dates: 24-25 April 2024
Conference Venue: Holiday Inn Potts Point, Sydney, Australia
Appears in: MATTER: International Journal of Science and Technology (ISSN 2454-5880)
Publication year: 2024

Achraf El Bouazzaoui et.al 2024

Volume 2024, pp. 53-54

DOI- https://doi.org/10.20319/icstr.2024.5354

This paper can be cited as: Bouazzaoui, A.E., Mouhib, O., Hadjoudja, A. (2024). Configurable Naive Bayes Implementation on FPGA Using Partial Reconfiguration. EnSci Sydney 2024 – International Conference on Engineering & Sciences, 24-25 April. Proceedings of Scientific and Technical Research Association (STRA), 2024, 53-54.

CONFIGURABLE NAIVE BAYES IMPLEMENTATION ON FPGA USING PARTIAL RECONFIGURATION

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Abstract

The Naive Bayes classifier is a fundamental algorithm in machine learning, known for its simplicity and effectiveness in various predictive modeling scenarios. However, its deployment in real-time applications demands efficient hardware implementations that can adapt dynamically to varying computational needs and model specifications. This work presents a novel FPGA-based implementation of Naive Bayes classifiers that leverages partial reconfiguration to enhance flexibility and resource efficiency. Our method employs a modular architecture that allows seamless switching among various Naive Bayes models, such as Gaussian, Multinomial, and Bernoulli, enhancing system flexibility without halting ongoing processes. By utilizing partial reconfiguration, our implementation minimizes the FPGA resource utilization, enabling

more efficient use of hardware. We thoroughly evaluate our system, focusing on reconfiguration time and resource efficiency. We demonstrate that our approach provides the operational flexibility needed for real-time data processing tasks, enabling quick adaptation to variable data types and distributions without interrupting ongoing processes. This adaptive framework supports dynamic scenarios, facilitating immediate updates in response to evolving conditions with minimal downtime.

Keywords

FPGA, Machine learning, Naïve Bayes, FPGA Accelerator