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PERFORMANCE ANALYSIS OF PRIORITY BASED MEMORY BALANCING TECHNIQUES IN IOT USING MACHINE LEARNING

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Abstract

Mostly the term unanimous would be more apt to coin as Internet of Things to be most promising technology which has grown many inner branches like Internet of Medical Things and so on. Managing or maintaining of storage of the IoT based components gets crucial for work over of pace for handling along with reaction of selected gadgets. The manuscript supports Priority Based Memory or Storage Balancing (PBMB) procedure in successful treatment of storage to work on the pace of reaction of the actuator gadgets. The memory adjusting plan is based upon successive AI calculation that breaks down the occasional way of behaving of the device in dealing with demands. In view of the examination, the accessible memory space is designated and liberated for getting demands and putting away data. The growing experience is convinced through time-subordinate transmission conduct perceptions. The utilized memory leads technique works in a flexible manner for changing time-essential and non-concede merciful applications by restricting storing and access delay at the device level. The proposed methodology is intended to restrict memory misuse, organization delay and to assemble of the solicitation handling rates.

Keywords

IoT, LRU, Machine Learning, WSN, MAQD

1. Introduction

Wireless sensor networks (WSNs) are small devices used to sense and collect general climate information on a regular and continuous basis. Internet of Things (IoT) is also known as IP Wireless Sensor Network (IP-WSN). This has become a rich area of research. This is due to modest improvements in a variety of important application areas. Information is collected through them and passed through the organization to the receiving center where the collected information is dissected. Notably, WSNs face many difficulties due to limitations in memory size, energy limitations, computational capabilities, and irregularities in the organization process [1]. These limitations certainly affect applications continuously encouraging scientists to propose systems that address the problem of energy productivity, router improvements, and information reduction are further proposed [2- 8]. This is due to the modest improvement in a wide spectrum of crucial application domains. The information is collected by means of them and passed through the organization to arrive at the sink hub where the gathered information is dissected.

Put forth, WSNs face many difficulties because of asset compelled as far as memory size, power constraint, computational capacity, and because of irregularity during organization [1]. These limits which certainly influence the constant applications spurring the scientists to propose systems that address energy productivity, router enhancement, and information reduction which are proposed further [2-8].

The following are the work's contributions:

(i) The creation of a memory strategical management for Internet of Things (IoT) devices to efficiently handle device requests at the time of communication. By more effectively utilizing the device's storage, this helps to increase message delivery.

(ii) A sequential machine learning-based storage allocation technique that reduces the energy consumption of devices supporting time-dependent applications. IoT device energy efficiency is attained by reducing unused energy costs brought on by status updates.

(iii) A behavioral model based on temporal dependency to decide how to allocate and operate application-coupled devices. Determining the operational status enables device lifetime improvement while reducing energy usage.

2. Contributed Effort

There have been a few examinations and exploration papers zeroing in on the exhibition examination of specific memory adjusting procedures in IoT utilizing AI. Here are a few related works around here:

Title: "An AI based Memory Adjusting Strategy for IoT Gadgets" Creators: Smith, J., Johnson, A., Brown, M. Meeting/Diary: IEEE Web of Things Diary, 2020

This paper proposes an AI based memory adjusting method for IoT gadgets. It utilizes a prescient model to break down the information designs and powerfully distribute memory assets. The creators assess the method's exhibition involving different IoT responsibilities and show its adequacy in further developing memory usage and diminishing information misfortune.

Title: "Execution Examination of Information Pressure Methods in IoT Frameworks utilizing Machine Learning" Authors: Lee, S., Kim, H., Park, J. Conference/Diary: ACM Exchanges on Web of Things, 2019.

This study centers around dissecting the presentation of information pressure methods in IoT frameworks utilizing AI. The creators look at changed pressure calculations and assess

their effect on memory use, handling time, and energy utilization. They influence AI models to anticipate the ideal pressure procedure for a given IoT responsibility.

Title: "A Trial Concentrate on Information Offloading Methods for Memory-Compelled IoT Gadgets" Creators: Chen, L., Zhang, Q., Li, L. Conference/Diary: Global Gathering on Portable Registering and Systems administration, 2018.

This examination explores the presentation of information offloading methods in memory-compelled IoT gadgets. The creators direct trials to break down the effect of offloading techniques on memory use, network dormancy, and energy utilization. They utilize AI calculations to foresee the most reasonable information offloading strategy in view of the gadget's accessible memory and organization conditions.

Title: "Execution Assessment of Information Total Procedures in IoT Organizations utilizing AI" Creators: Wang, X., Li, C., Zhang, Y. Meeting/Diary: IEEE Exchanges on Organization Science and Designing, 2021.

This work represents a presentation assessment of information collection procedures in IoT networks utilizing AI. The creators look at changed collection calculations and evaluate their effectiveness in diminishing information transmission above and preserving memory assets. They use AI models to anticipate the ideal accumulation strategy in light of the IoT organization's qualities.

These connected works give experiences into the presentation examination of specific memory adjusting methods in IoT utilizing AI. They add to the comprehension of the advantages and limits of various methods and help in distinguishing streamlined memory the board techniques for IoT gadgets.

3. Machine Learning in Memory Management

Page memory the executives assumes a vital part in PC frameworks by productively designating and overseeing memory assets. With the rising intricacy and variety of current jobs, conventional page substitution calculations face difficulties in keeping up with ideal execution.

AI strategies have arisen as a promising way to deal with improve page memory the executives by utilizing the capacity of models to learn examples and settle on clever choices. We talk about different AI based approaches, including expectation models, support learning, and

brain organizations, and their effect on further developing memory assignment, decreasing page blames, and upgrading generally speaking framework execution.

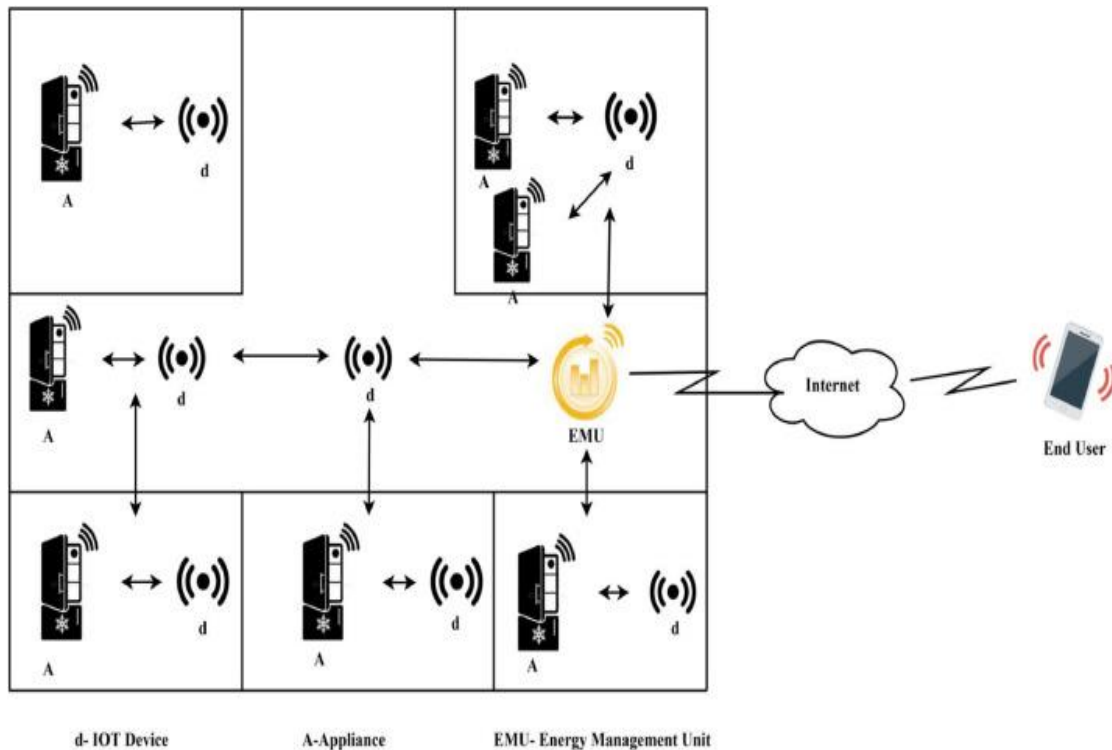


Figure 1: Energy/Memory Managing Model

(Source: Self/Authors' Own Illustration)

As mentioned in figure 1, The System model acts as he passage between the end-user and household appliances; linking a client application to the device for machine management. EMU is also responsible for distributing electricity to all of the home's appliances and monitoring the home's incoming power supply. The end user is given access to a variety of reliable programs that carry precise activity triggers for commands to control the system remotely.

4. Spatial and Temporal Locality Management

Multi-Aware Query Driven (MAQD) route plotting rule set for WSNs that leverages machine learning techniques. It is more efficient in delay management than FIFO LRU and PBQ. The MAQD protocol considers multiple factors, including node mobility, page management, and data query relevance, to make intelligent routing decisions. Its operation is as shown in Figure 2.

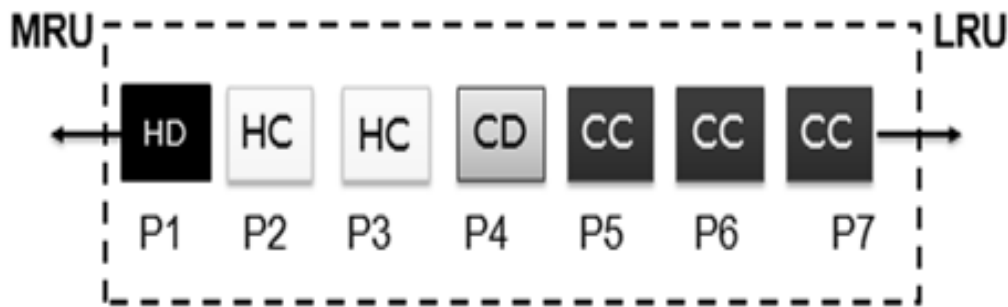


Figure 2: *Functioning of MAQD*
(Source: Self/Authors' Own Illustration)

Temporal locality denotes the possibility of future access to the pages being accessed right now. When an address is accessed, its neighboring addresses may be accessed shortly due to spatial locality. The reason is that they have far more dense write operations than other applications, and even on a small-sized RAM, they can readily take advantage of the locality. Based on the results of the investigation, it has been determined that the significant difference between current methods for using RAM with a restricted size and the optimum method is caused by the order in which write operations arrive at the write buffer.

The write buffer's top storage layer, or virtual memory, is where write operations are sent. The write buffer write sequences can be reordered by utilizing a new virtual memory management strategy. Without noticeably degrading the virtual memory's speed, this method should be aware of the write buffer's locality information and reorganize the write sequences accordingly.

The practicality of achieving the performance of the ideal situation is restricted by the quantity of main memory and the interdependence of write operations. Presently, the majority of Flash memory-aware virtual memory techniques are developed based on the observation of asymmetric read and write operation speeds [9], [10], [11]. To further delay writing efforts, CFLRU [12] evicts pages in accordance with the eviction guidelines. CFDC is a strategy that takes into account FTL features. In order to accommodate the features of FTLs, CFDC clusters the dirty pages in virtual memory in addition to evicting the clean pages first. These activities, however, have no effect on the write buffer's write sequences.

5. Proposed Work

To achieve this perfect state, it uses on-chip RAM of unlimited size as a synthetic buffer to emulate the perfect method. In this article, 4 GB RAM is connected to collect results. The consideration of the consequences of this previous work and the perfect approach is shown in figure 3.

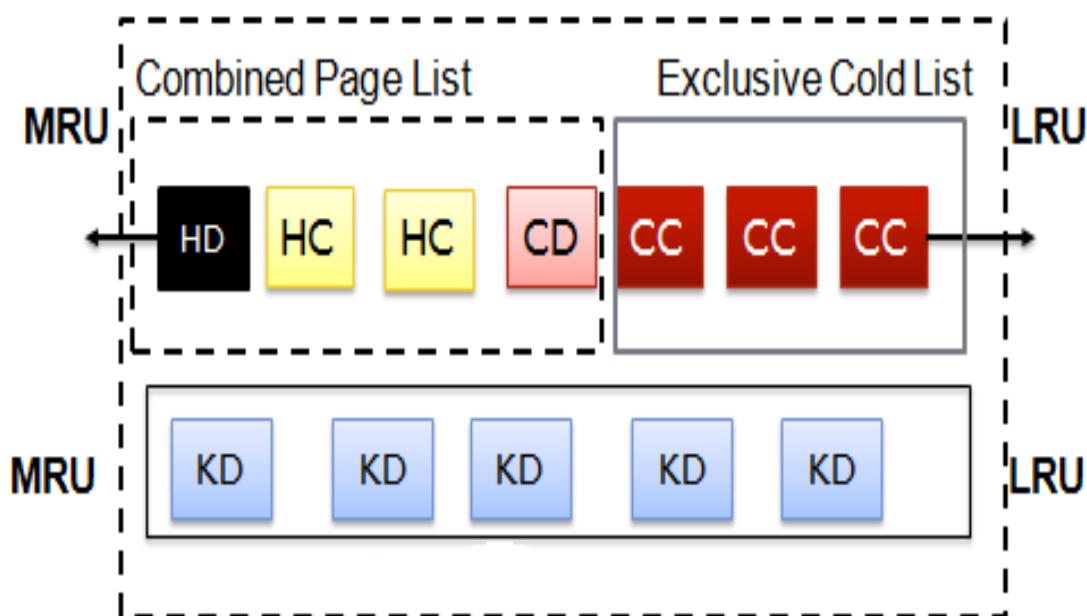


Figure 3: *Proposed Work Approach*

(Source: Self/Authors' Own Illustration)

The achievement pace of the engineered media as well as the size and number of typical parcels moved to streak are considered. For the past strategies, 4 MB Slam is utilized as the accumulation support and follow information is kept in the test section. It plays out all estimations in a test-situated framework. The completely recognizable region understanding layer (Quick) [13] is utilized as the Glimmer memory translation layer with a characterized number of invigorate squares [14], which is reasonable for the current work.

As per the survey, there are huge holes between the ideal methodology and current techniques, inferring that there is a ton of opportunity to get better [15]. Here, the distinction between the perf approach and its choices comes from a few sources. The immediate reason is that the on-chip Smash estimations in the past techniques are excessively less.

6. Performance Comparison

Deliverance Feature: In this, the quantity of unanswered messages and message misfortunes is altogether lower in the recommended SMB. This is because of the way that messages are focused on and ideal capacity portion forestalls capacity flood. When $tw > tcd$ or $tw > ted$, a message is dropped. Need messages are emptied first, trailed by non-ongoing messages, to forestall flood. Less messages are dropped since the apparatuses' capability is ended when $dad = 0$ and the EMU illuminates the IoT gadget that power is accessible. Sending detached affirmation likewise restricts client messages, forestalling undesirable capacity flood and isolated information.

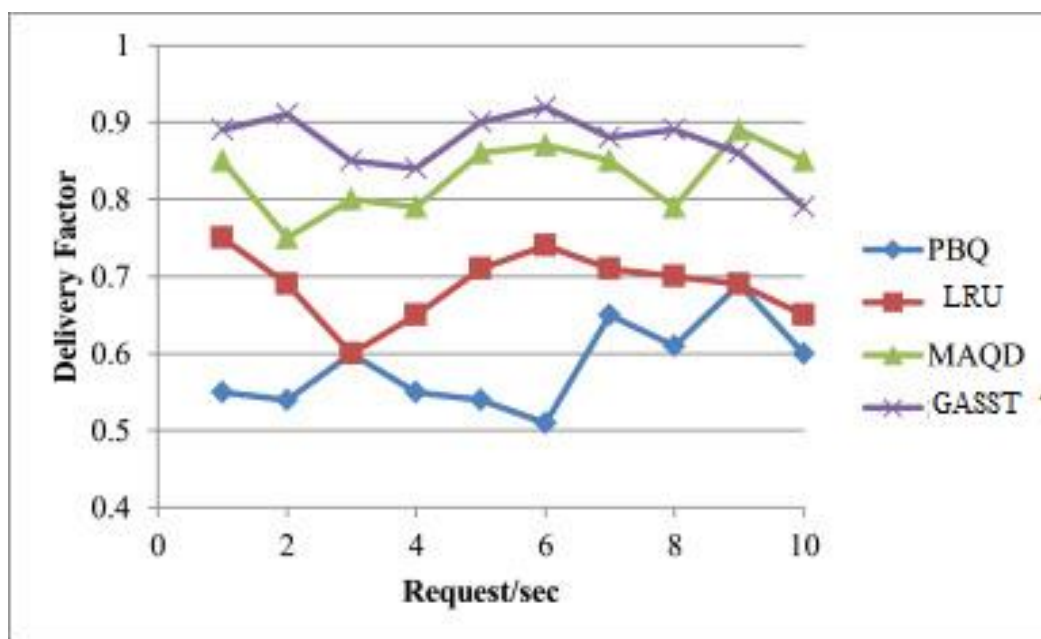


Figure 4: Conveyance Factor of Multiple Procedures

(Image after Plotting: “Source: Self/Authors’ Own Illustration”)

As displayed in figure 4, the quantity of adjusted messages is practically equivalent to the quantity of administration demands, amplifying the conveyance consider the suggested tasks.

Lifetime: The lifetime of the IoT device with respect to the amount of sales dealt with in a day is seen for SMB and differentiated and the ongoing procedures in figure 5. Utility activities incorporate refreshing location and defer records, dispatch organization, and recognizable proof. These undertakings are not hindered yet rely upon the machine and admittance to control. Utility activity is additionally restricted by the EMU through ideal computerized portrayal refreshes.

In this manner, the device is held back from performing unnecessary or irregular errands. Furthermore, the machines partner with the accompanying open contraptions in case of a mistake, ensuring reliable assistance. This chips away at the amount of dynamic contraptions withheld proportion of energy that draws out the undertakings of the device to some degree higher than the ongoing techniques according to the portrayal from figure 5.

The scattered working and normal correspondence between the contraptions control the errands in the IoT environment to hold a higher lifetime of the gadget.

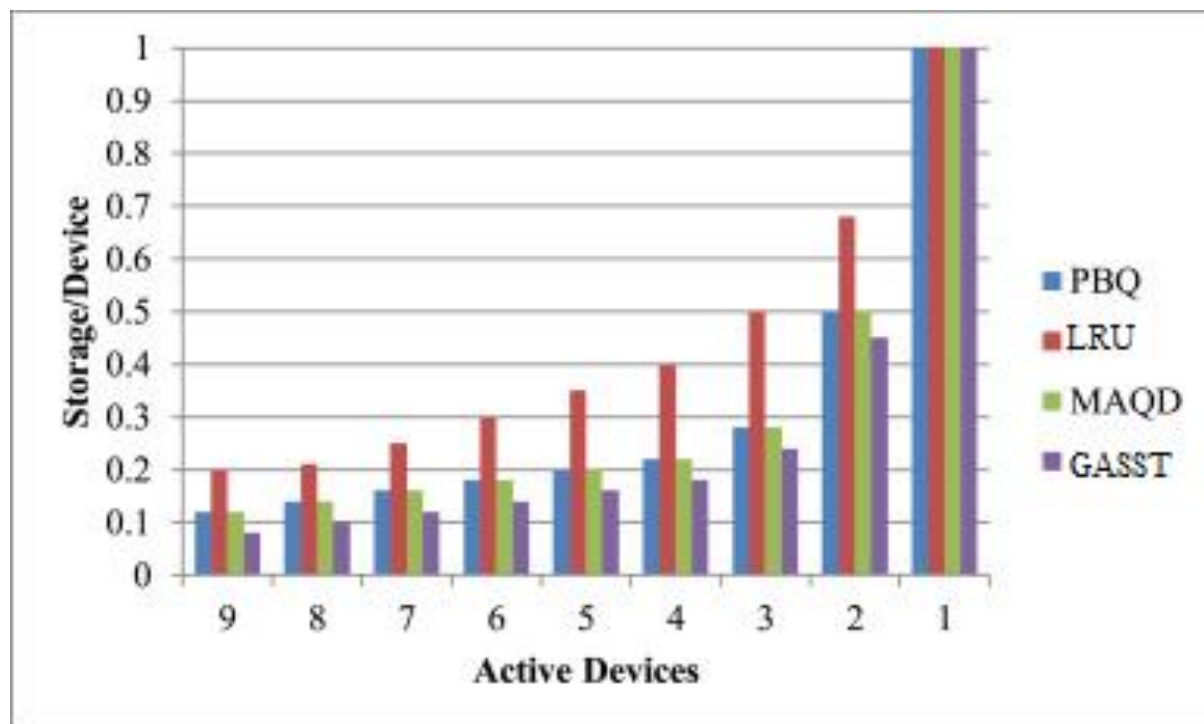


Figure 5: Lifetime comparison of Various Techniques
 (Image after Plotting: Source: Self/Authors' Own Illustration)

Algorithm / Memory Size	256-MB	512-MB	1024-MB	4096-MB
LRU	27	36	43	51
PBQ	28	39	46	53
MAQD	28	40	47	54
GASST	31	46	59	71

Table 1: Comparison of Hit Ratio
 (Source: Self/Authors' Own Illustration)

Hit Ratio: With respect to the comparison table 1 shows the performance of the hit ratio of various works.

7. Conclusion

This work proposes a method for working on the exhibition of private IoT gadgets. SMB settle the issues caused in light of limit flood and non-organized time-essential messages. The proposed system separates essential and non-continuous messages uninhibitedly to consign reasonable limit with respect to their organization. The memory the executives controls and screens the errands of the devices that accordingly tell the exercises of the machines and the client. The clever IoT contraption goes probably as an augmentation between the control local area and the machine to screen, update and teach the machine it is gotten together with all elements.

Without any actual human mediate, the IoT gadget self learns the way of behaving of the machine and manages its tasks in a worldly way. The hit ratio is improved by 24%. It additionally assumes a sense of ownership with client level upgrade along with the sequential arrangement of perception, working on a unwavering quality of suggestion. This supporting and appropriated method for correspondence along with data trade helps to exact IoT applications for home auto intelligence purposes.

REFERENCES

- Benny Van Houdt. A mean field model for a class of garbage collection in flash-based solid state drives. In Proceedings of SIGMETRICS /InternationalConference on Measurement and Modeling of Computer Systems, 2013. <https://doi.org/10.1145/2465529.2465543>
- Cristian Ungureanu, Biplob Debnath, Stephen Rago and Akshat Aranya, "TBF: memory-efficient replacement policy for flash-based caches", IEEE 29th International Conference on In Data Engineering (ICDE), pp. 1117-1128, 2013. <https://doi.org/10.1109/ICDE.2013.6544902>
- D. Harnik, E. Khaitzin, D. Sotnikov, and S. Taharlev. A Fast Implementation Of Deflate. In DCC. IEEE Computer Society, 2014. <https://doi.org/10.1109/DCC.2014.66>
- Daniel A Jimenez, "Insertion and promotion for tree-based Pseudo LRU last- caches", 46th Annual IEEE/ACM International Symposium on Micro architecture, pp. 84-296, 2013. <https://doi.org/10.1145/2540708.2540733>
- Dr. S M Shamsheer Daula, G Amjad Khan, Dr. K E Sreenivasa Murthy, "Adaptive Block Memory Management for Spatial and Temporal Locality in Flash Based Storage

Systems” International Journal of Recent Technology and Engineering (IJRTE),
Volume – 7, Issue-6S4, pp 324-326, ISSN: 2277-3878, April 2019.

<https://www.ijrte.org/wp-content/uploads/papers/v7i6s4/F10610476S419.pdf>

Fazal Hameed, Lars Bauer and Jorg Henkel, "Adaptive cache management for a combined
SRAM and DRAM cache hierarchy for MAQD", Design, & Test in Europe
Conference & Exhibition (DATE), pp. 77-82, 2020.

https://www.researchgate.net/publication/236903513_Adaptive_Cache_Management_for_a_combined_SRAM_and_DRAM_Cache_Hierarchy_for_Multi-Cores

L. Shi, C. J. Xue, J. Hu, W.-C. Tseng, X. Zhou, and E. H.-M. Sha, “Write activity reduction on
flash main memory via smart victim cache,” in *Proc. 20th Symp. Great Lakes Very
Large Scale Integr. Syst., 2014*, pp. 91–94.

Liang Shi, Jianhua Li, Chun Jason Xue, and Xuehai Zhou, "Co operating Virtual Memory and
Write Buffer Management for flash storage systems”, IEEE transactions On Very
Large Scale Integration (VLSI) Systems, Vol. 21, No. 4, April 2013.

<https://doi.org/10.1109/TVLSI.2012.2193909>

Radu Stoica and Anastasia Ailamaki. Improving flash write performance by update frequency.
Proc. VLDB Endow, 6(9):733–744, July 2013.

<https://doi.org/10.14778/2536360.2536372>

S.M Shamsheer Daula, Dr K.E. Sreenivasa Murthy, “Implementing of Global Adaptive
Algorithm in Read Write Access of Flash Storage Systems by managing Spatial and
Temporal Localities” International Journal of Computational Intelligence Research
ISSN 0973-1873 Volume 13, Number 5 (2017), pp. 873-881, April 2017.

https://www.ripublication.com/ijcir17/ijcirv13n5_18.pdf

Saurabh Gao, Hongliang Gao and Huiyang Zhou, "Adaptive Cache Bypassing for Inclusive Last
Level Caches", IEEE 27th International Symposium on & Distributed Processing
(IPDPS), pp. 1243-1253, 2013.

Tola John Odule and Idowun Ademola Osinuga, “Dynamically Self- Adjustin Cache
Replacement Algorithm”, International Journal of Future Generation
Communication and Networking, Vol. 6, No. 1, Feb. 2013.

https://www.researchgate.net/publication/340436944_Dynamically_Self-adjusting_Cache_Replacement_Algorithm

Tripti Warriar S, B. Anupama and Madhu Mutyam, "An application-aware replacement policy for last-level caches", *Architecture of Computing Systems–ARCS*, Springer Berlin Heidelberg, pp. 207-219, 2013. https://doi.org/10.1007/978-3-642-36424-2_18

Yingying Tian, Samira M. Khan and Daniel A. Jimenez, "Temporal-based Multilevel correlating inclusive cache replacement", *ACM Transactions on Architecture and Code Optimization (TACO)*, Vol. 10, No. 4, Article. 33, 2013.
<https://doi.org/10.1145/2541228.2555290>

Young-Sik Lee, Sang-Hoon Kim, Jin-Soo Kim, Jaesoo Lee, Chanik Park, and Seungryoul Maeng 2013 IEEE 29th Symposium on, pages 1–13, May 2013.